INSTRUCTION MANUAL

MODEL 5107
FREQUENCY SYNTHESIZER
CHANNEL

WAVETEK
SAN DIEGO

9045 BALBOA AVENUE, SAN DIEGO, CALIFORNIA

INSTRUCTION MANUAL

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SECTION I

GENERAL INFORMATION

1-1. Introduction

The Model 5107 Frequency Synthesizer Channel generates spectrally pure and stable output frequencies from 1 Hz to 3 MHz with constant 1 Hz resolution. It utilizes a unique direct digital synthesis technique* to generate the output sinusoid. Complementary TTL compatible square wave outputs are provided for monitoring the output of the channel.

The Model 5107 Frequency Synthesizer Channel obtains its input power, clock, control logic, and programming information externally. The purpose of this manual is to supply the necessary information to operate the Model 5107 Frequency Synthesizer Channel as a stand-alone assembly.

1-2. Theory of Operation

The Model 5107 utilizes direct digital synthesis techniques to generate the output sinusoid. Samples of the sinusoid are digitally generated at an 8 MHz rate and are then converted to analog form by a digital-to-analog converter (DAC) and a smoothing, low pass filter which cuts off at approximately 3.5 MHz. The amplititude of the digital samples is represented by 11 bits (including sign). A block diagram of the Model 5107 is given in Figure 1. The frequency stability and accuracy of the output sinusoid is related directly to the system clock.

The frequency of the output signal is stored in a frequency register which can, on command, transmit its programmed data back over the 22 programming lines. The register stores the frequency in a modified binary form, with both 3-decade groups (Hz and KHz) represented by separate 10-bit words. The two MHz bits appear as two bits on the most significant end of the KHz word, making it 12 bits in length. This data is presented to a phase accumulator whose rate of phase accumulation is directly proportional to its input. The phase accumulator output is a linearly increasing binary equivalent of $0\text{-}90^{0}$. A read-only memory (ROM) has programmed in it the appropriate sine function value for each phase angle address. By proper use of data complementing at the input and output of the ROM, the entire sinusoidal cycle can be produced.

*U.S. Patent No. 3,735,269

1-2. Theory of Operation - continued

The output of the ROM, which is now an 11-bit binary word, is converted to staircase-waveform approximation of a sinusoid by a digital-toanalog converter (DAC). The low pass filter smooths the sinusoid to the rated spectral purity. Since 11 bits of the phase resolution are used, the phase accuracy of each converted sample deviates no more than $\pm 0.09^0$ from a pure sinusoid. The low pass filter output is then fed to an output amplifier. A squaring circuit also derives its input from the output amplifier and provides two complementary TTL-compatible outputs.

Also contained within the Model 5107 Synthesizer is the control logic which interfaces the synthesis and program load/read facilities.

1-3. Specifications

OUTPUT FREQUENCY RANGE: 1 Hz to 2,999,999 Hz

FREQUENCY RESOLUTION: 1 Hz throughout entire range

OUTPUT SIGNALS:

SINEWAVE OUTPUT #1: Fixed amplitude, 1.5 volts RMS $\pm$ 0.5 dB from 1 Hz to 1 MHz and + 0.5 dB - 2.5 dB from 1 MHz to 3 MHz with 50-ohm source impedance

SPURIOUS COMPONENTS: (see CAUTION below) Harmonic components do not exceed -40 dB. Non-harmonic components typically do not exceed -50 dB from 1 Hz to 2MHz and -40 dB from 2 MHz to 3 MHz

PHASE NOISE: (see CAUTION below) Phase noise in 30 KHz band excluding 1 Hz centered on carrier does not exceed -50 dB from 1 Hz to 2 MHz and -40 dB from 2 MHz to 3 MHz

SQUARE WAVE OUTPUT #2: TTL level capable of driving 30 standard TTL loads. Same phase noise specification as Output #1.

SQUARE WAVE OUTPUT #3: TTL level capable of driving 30 standard TTL loads, complementary to Output #2. Same phase noise specification as Output #1.

FREQUENCY CONTROL: Output frequency may be selected via a 22-bit parallel binary word, and the programmed frequency may be read out over the same bus.

PROGRAMMING DELAY: 2 sec max with amplitude and phase continuity maintained between any two programmed frequencies.

UPDATE RATE: Programmed frequencies may be updated at 0.125 sec intervals.

INPUT SIGNALS: Requires 8 MHz Reference Oscillator Clock (TTL). Input loading is one standard TTL load.

INPUT POWER: Requires regulated +5VDC at 2.5 Amps and $\pm$ 15 VDC at 100 mA

TEMPERATURE: 0^0C to $+50^0$C operating, -20^0C to $+70^0$C non-operating

DIMENSIONS: 8.75" high x 1.35" wide x 13.545" deep

MATING CONNECTORS: Programming mating connectors: Amphenol #205514-1 Sinewave output #1: Sealectro #52-610-9237-99

CAUTION

The specifications on spectral purity (Spurious components and phase noise) are applicable when Model 5107 Frequency Synthesizer Channel is contained where adequate shielding, crystal reference input, power supplies and programming lines have been provided.

Proper arrangements must be made to assure sufficient air flow around and through Model 5107 when it is mounted in its enclosure.

SECTION II

OPERATION

2-1. Introduction

The Model 5107 Frequency Synthesizer Channel when used as a standalone assembly requires power, an 8 MHz reference clock, programming data and control signals.

2-2. Interface Description

A description of the programming connector can be found in Table 1. The following is a description of this interface.

1. POWER: + 5 VDC at 2.5 amps; $\pm$ 15 VDC at 100 mA.

2. INPUT REFERENCE: 8MHz Reference Clock, TTL, duty cycle approximately 50%. It is recommended that this input be transmitted via coax cable. The frequency limits of the signal are from DC to 8.1 MHz. The deviation of the frequency of the output signal (the programmed frequency) is directly proportional to the deviation for the external clock from 8 MHz. Operation at frequencies below 8MHz results in a lower sampling rate; the internal low pass filter which removes sampling components from the output signal is designed for an 8 MHz sampling rate and becomes less effective as the sampling rate is lowered. To maintain full harmonic and spurious distortion specifications, an external low pass filter is required to eliminate these components. Cutoff frequency of this filter should be slightly above highest output frequency.

3. PROGRAMMING DATA (A0 TO A21): The frequency programming lines are bidirectional. The Model 5107 frequency programming interface is a tri-state TTL bus and should be driven with open collector or tristate devices. To program a given frequency, verify proper logic states of the control lines (Section 2-2-4). The weight of each program line is shown in Table 1. Positive logic is used: a logical "1" on any line will cause a contribution to the frequency equal to the weight of that line. Any binary number less or equal to 999_{10} = $11111\ 00\ 111_2$ is valid for each of the two frequency ranges (Hz and KHz). When the Model 5107 Frequency Synthesizer Channel is interrogated (refer to Section 2-2-4 for the appropriate logic levels on the control lines), the stored programmed information is transmitted over the programming lines. A logic "1" indicates a contribution equal to the weight of the line.

2-2. Interface Description - continued

4. CONTROL LINES

A) Enable - low active - when more than one Model 5107 is used in a system, this line allows selection of a specific unit for participation in loading and reading frequency commands from a common control bus. Only one unit should be enabled at any time. When the Model 5107 is used as a stand-alone synthesizer, this line sould be tied to ground. A logic "0" on this line is required in order to load frequency data or read stored frequency data.

B) Read - low active - a logic "0" on this line allows the Model 5107 to transmit the programmed frequency over the frequency programming lines (provided the enable line is low). If the Model 5107 is not to be interrogated, this line should be held high.

C) Load - low active - a logic "0" on this line allows the Model 5107 to be programmed to the frequency information contained on the programming lines (provided the enable line is low).

NOTE: The Read and Load lines should NOT be held low simultaneously.

5. ZERO PHASE LINE

By setting a logical "0" on this line, the internal sample generator is reset to the zero-phase state causing the output signal to go to zero volts DC. When this line is set back to logical "1", the output waveform resumes at the zero-phase point. The minimum duration of the logical "0" interval is 125 nsec, and there is approximately 1.5 sec delay to the OUTPUT jack.

6. STATUS LINES

A) Acknowledge - low active - transmitted on a tri-state bus. A logic "0" indicates the Model 5107 Frequency Synthesizer Channel has been enabled and a frequency was loaded.

B) Presence - low active - transmitted on a tri-state bus. A logic "0" indicates the Model 5107 Frequency Synthesizer Channel has been enabled.

7. TEST POINTS

A) Hz Carry - test point for verification of proper operation of the accumulator section. Should be left open.

B) KHz Carry - test point for verification of proper operation of the accumulator section. Should be left open.

C) Sign Bit - test point. Should be left open.

2-3. Example of Model 5107 Programming

To program the Model 5107 to 2,500,010 Hz, the following must be performed:

1. Supply + 5 VDC, + 15 VDC and - 15 VDC as per Table 1.
2. Supply a 8 MHz clock as per Table 1.
3. Leave the Hz Carry, KHz Carry, Zero Phase lines open.
4. Set the Enable line to a logic "0" (low). (The presence line will go to logic "0".)
5. Set the Read line to a logic "1" (high).
6. Set the following lines to a logic "1": 2 MHz (pin M), 256 KHz (pin $\overline{A}$), 128 KHz (pin $\overline{E}$), 64 KHz (pin $\overline{K}$), 32 KHz (pin $\overline{H}$), 16 KHz (pin $\overline{C}$), 4 KHz (pin U), 8 Hz (pin $\overline{D}$), and 2 Hz (pin V).
7. Set the follwing lines to a logic "0": 1 MHz (pin S), 512 KHz (pin W), 8 KHz (pin Y), 2 KHz (pin P), 1 KHz (pin N), 512 Hz (pin T), 256 Hz (pin X), 128 Hz (pin $\overline{B}$), 64 Hz (pin $\overline{F}$), 32 Hz (pin $\overline{M}$), 16 Hz (pin $\overline{J}$), 4 Hz (pin Z), and 1 Hz (pin R).
8. Set the load line to a logic "0". This line must be low at the same time the 8 MHz clock is low in order to load the frequency settings. (The Acknowledge line will go low, indicating the data has been loaded).

In order to read the information contained on the programming lines, the following must be performed:

1. Repeat 1, 2, 3 and 4 above.
2. Set the Load line to a logic "1".
3. Set the Read line to a logic "0".
4. Monitor the logic levels on the frequency programming lines (A0 through A21). Lines with a logic "1" indicate that the weight of that line is contributing to the output frequency.

2-4. Model 5107 Frequency Synthesizer Channel Timing Information

The timing diagram for the Model 5107 channel can be found in Figure 2. Following is a description and specification of these times:

		Min	Max
t_0	Setup time ENABLE to READ	0	-
t_1	Delay time from READ to DATA VALID	-	50 nsec
t_2	Delay time from READ to DATA INVALID	0 nsec	-
t_3	Hold time from ACLK to LOAD	10 nsec	-
t_4	Setup time from LOAD to ACLK	10 nsec	-
t_5	Hold time from ACLK to LOAD	10 nsec	-
t_6	Setup time from LOAD to ACLK	10 nsec	-
t_7	Setup time from DATA VALID to ACLK	30 nsec	-
t_8	Hold time from ACLK to DATA VALID	10 nsec	-
t_9	Setup time from ENABLE to LOAD	10 nsec	-
t_{10}	$\overline{\text{ACLK}}$ pulse width (active low)	50 nsec	75 nsec

NOTES:

1. The A Bus must not be driven by controller whenever ENABLE and READ are active (low).

2. LOAD may be held active (low) for any number of $\overline{\text{ACLK}}$ cycles.

3. Data will be loaded on the low to high transition of $\overline{\text{ACLK}}$ when ENABLE and LOAD are active (low).

4. ENABLE may be used to disable LOAD and READ functions by setting ENABLE high. If ENABLE is tied low, then LOAD and READ will always be enabled.

5107 INTERFACE

PIN	DESCRIPTION	PIN	DESCRIPTION
A	5V GROUND	$\overline{D}$	8 Hz (A18)
B		$\overline{E}$	128 KHz (A4)
C	5V GROUND	$\overline{F}$	64 Hz (A15)
D		$\overline{H}$	32 KHz (A6)
E	HERTZ CARRY (HC)	$\overline{J}$	16 Hz (A17)
F	$\overline{\text{READ}}$	$\overline{K}$	64 KHz (A5)
H	$\overline{\text{ZERO PHASE}}$ ($\overline{\text{ZP}}$)	$\overline{M}$	32 Hz (A16)
J	SIGN BIT (SGN)	$\overline{N}$	$\overline{\text{ENABLE}}$ ($\overline{\text{EN}}$)
K	K HERTZ CARRY (KC)	$\overline{P}$	8 MHz CLOCK ($\overline{\text{ACLK}}$)
L	$\overline{\text{LOAD}}$	$\overline{R}$	
M	2 MHz (A0)	$\overline{S}$	8 MHz CLOCK RETURN ($\overline{\text{CLKR}}$)
N	1 KHz (A11)	$\overline{T}$	+15V
P	2 KHz (A10)	$\overline{U}$	-15V
R	1 Hz (A21)	$\overline{V}$	$\overline{\text{ACKNOWLEDGE}}$ ($\overline{\text{ACKA}}$)
S	1 MHz (A1)	$\overline{W}$	GROUND ($\pm$15V)
T	512 Hz (A12)	$\overline{X}$	+15V
U	4KHz (A9)	$\overline{Y}$	-15V
V	2 Hz (A20)	$\overline{Z}$	$\overline{\text{PRESENCE}}$ ($\overline{\text{PRES}}$)
W	512 KHz (A2)	AA	GROUND ($\pm$15V)
X	256 Hz (A13)	BB	TTL OUTPUT #2
Y	8 KHz (A8)	CC	
Z	4 Hz (A19)	DD	+5V
$\overline{A}$	256 KHz (A3)	EE	TTL GROUND OUTPUT
$\overline{B}$	128 Hz (A14)	FF	+5V
$\overline{C}$	16 KHz (A7)	HH	$\overline{\text{TTL OUTPUT \#3}}$

TABLE 1
Model 5107 Frequency Synthesizer Channel
Remote Interface

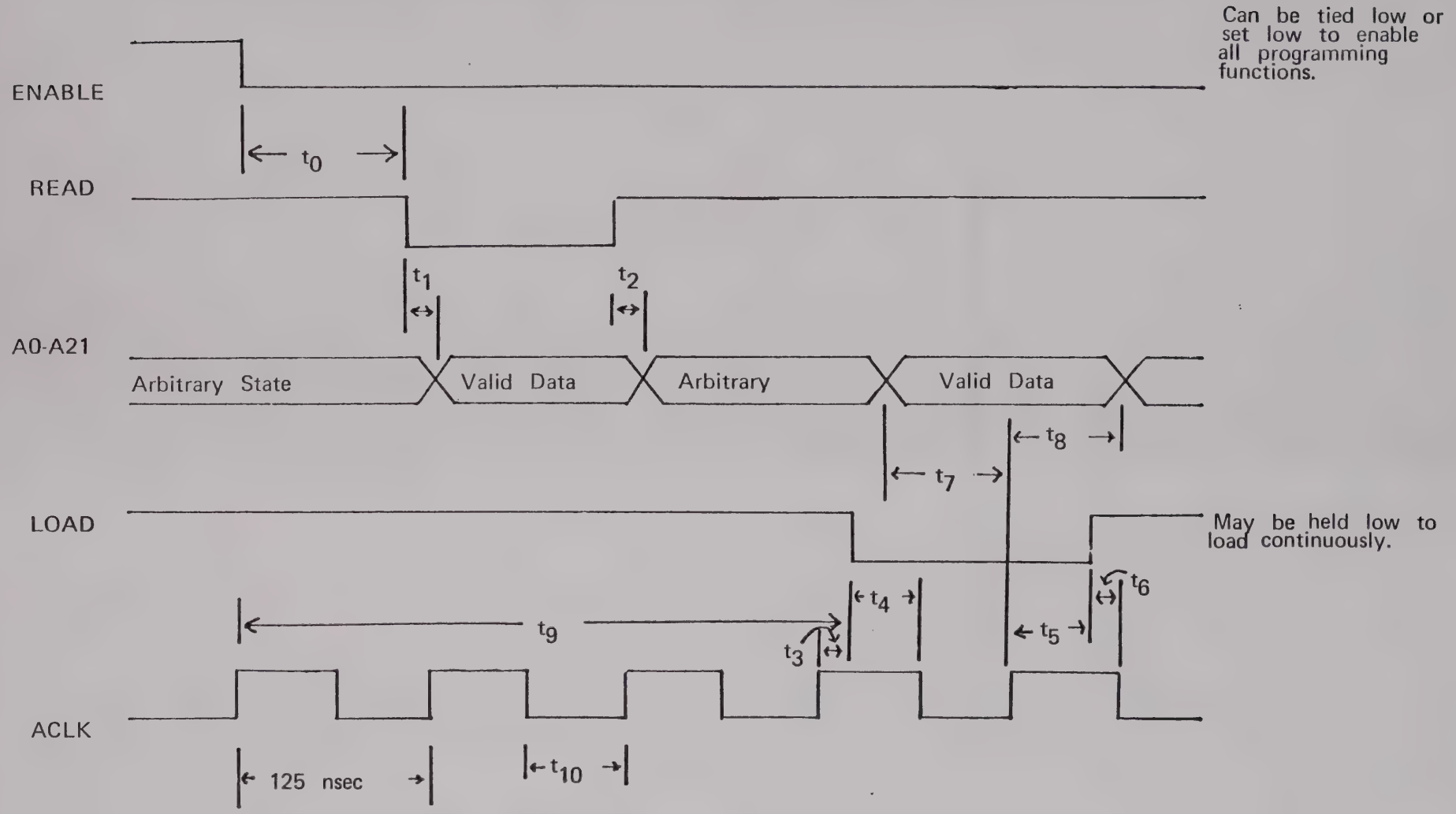
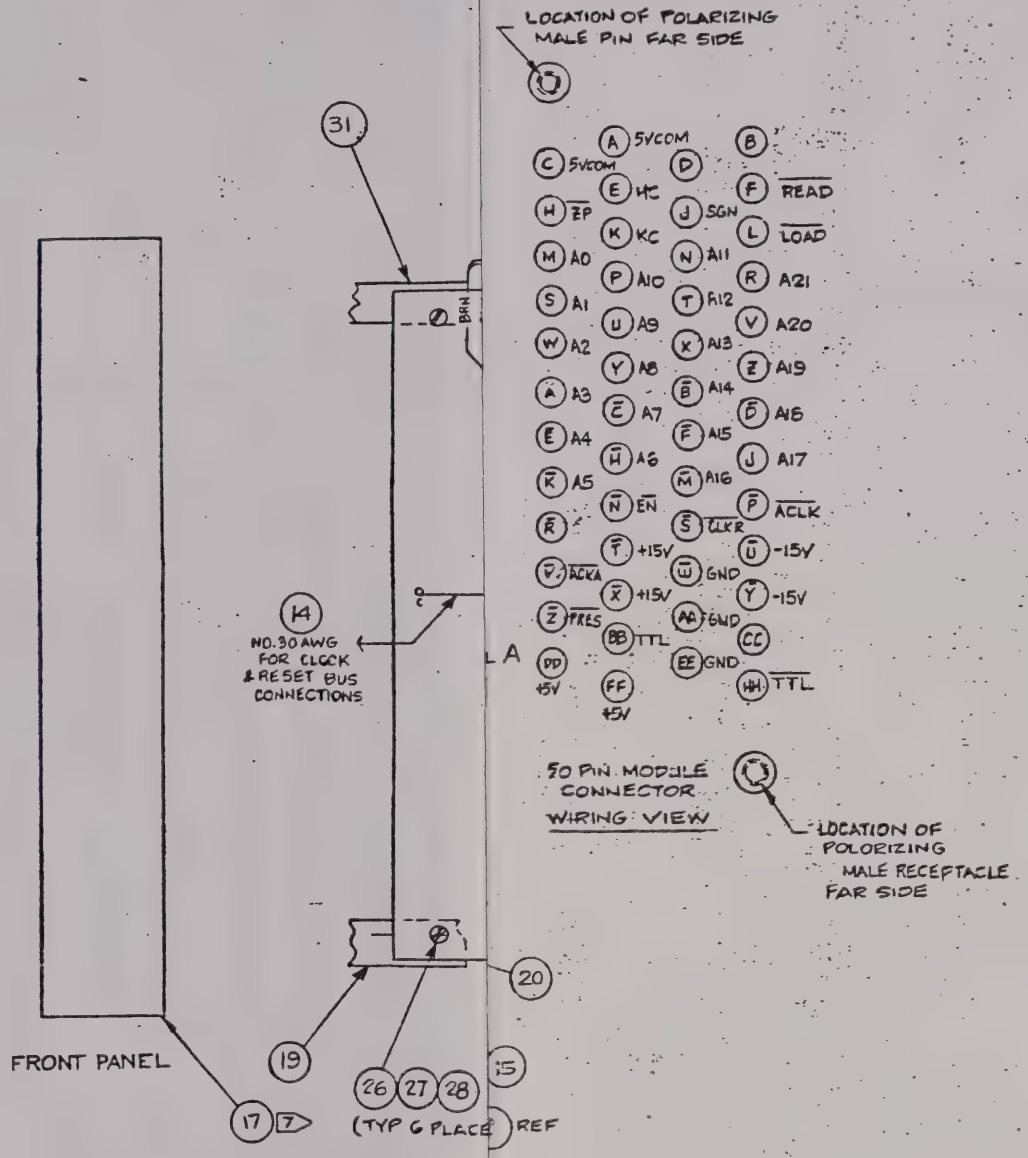


Figure 2
Timing Diagram

SECTION III

SCHEMATICS, ASSEMBLY PRINTS & PARTS LIST

LTR	ECO NO.	CHANGED BY	APPV'D BY	DATE
A	RELEASE			8/19/83
B	1698	NP 11/9/83		11/10/83



SHEETS 2 & 3 "A" SIZE P/L

DRAWN BY: R. Peters	DATE: 8/19/83	ROCKLAND Rockland Systems Corporation
CHECKED BY:		
ENG. APPVL:		
MFG APPVL:		

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE: .XXX ± .XX ± F/x ± 1/64 ∠° ± 1°

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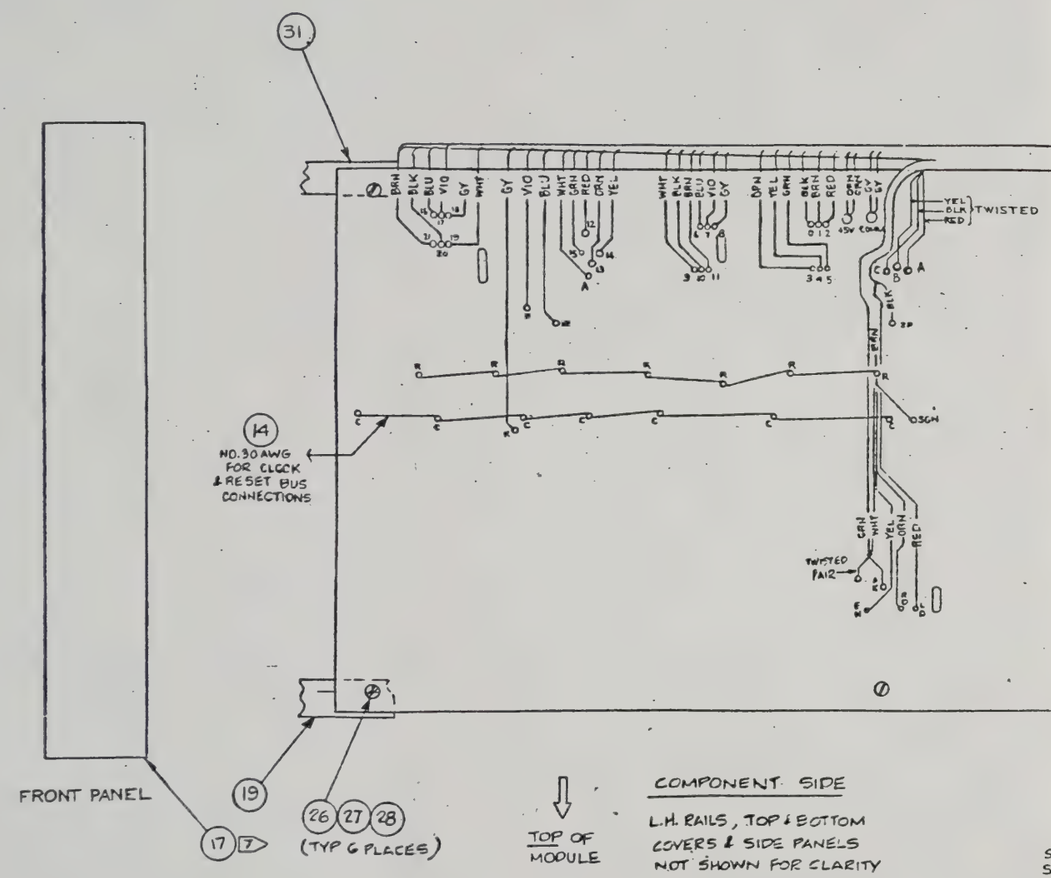
TITLE: MODULE CHASSIS 5107 (WIRING DIAGRAM & ASSY)

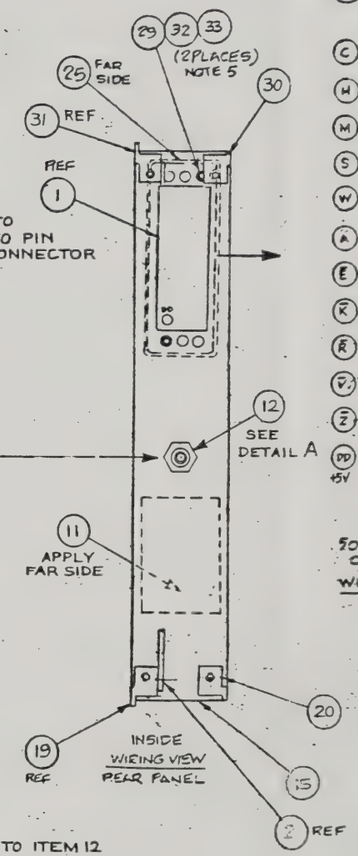
SIZE D | DRAWING NO. 02 002-3167 | REV B | SCALE 1/1 | SHEET 1 OF 3

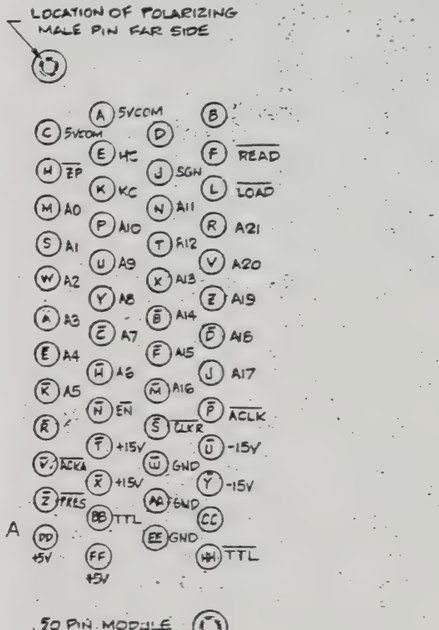
LTR	ECO NO	CHANGED BY	APPVD BY	DATE
A	RELEASE			11/9/83
B	1698	NP 11/9/83		11/11/83

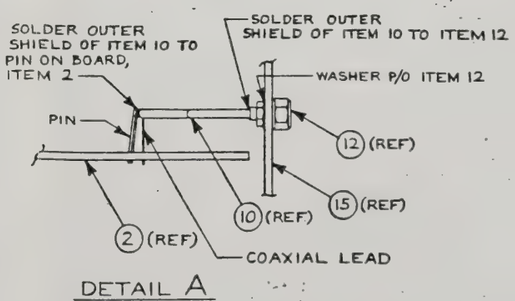
NOTES:

1. ASSEMBLE ITEM 1 TO 2. DO NOT PLUG IN 15V SUPPLY WIRES.
2. MOUNT ITEM 30 TO ITEM 15.
3. ASSEMBLE ITEM 2 TO ITEMS 19 & 31.
4. INSERT ITEM 1 THRU HOLE IN ITEM 15 & INSTALL HOOD ITEM 28. MOUNT ITEM 21 TO ITEM 15. INSTALL HARDWARE ITEMS 32, 33 & 29, ALIGN USING RODS & TIGHTEN HARDWARE.
5. MOUNT ITEM 20 TO ITEM 15.
6. MOUNT ITEM 17 TO ITEMS 19, 20, 30 & 31.








SOLDER OUTER SHIELD OF ITEM 10 TO PIN ON BOARD, ITEM 2
SOLDER OUTER SHIELD OF ITEM 10 TO ITEM 12
WASHER P/O ITEM 12
PIN
12 (REF)
15 (REF)
10 (REF)
2 (REF)
COAXIAL LEAD

DETAIL A

SHEETS 2 & 3 'L' SIZE P/L

DRAWN BY: L. Lefko	DATE: 9/30/83	ROCKLAND Rockland Systems Corporation
CHECKED BY: JW	10/4	Confidential property of ROCKLAND SYSTEMS CORP. not to be disclosed to others, reproduced or used for any purpose except as authorized in writing by above.
ENG APPVL: JM	9/30/83	
MFG APPVL: JW	10/4/83	

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TITLE: MODULE CHASSIS 5107 (WIRING DIAGRAM & ASSY)

SIZE D | DRAWING NO. 002-3167 | REV B | SCALE 1/1 | SHEET 1 OF 3

LEVEL 3

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Rockland Systems Corporation

TITLE MODULE CHASSIS 5107 ASSEMBLY

LIST OF MATERIAL 02 002-3167 REV B

RELEASE AUTHORITY CHIEF ENGR. RM QW ASSY SIZE D DATE 9-23-83 SHEET 2 OF 3

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
1	02-009-9167	1	CONNECTOR HARNESS ASSY	
2	02-004-3167	1	PWB ASSY CHANNEL 5107	
3	02-002-3167	REF	WIRING DIAGRAM	
4	389.7003	2	GUIDE PIN ASSY, MALE	AMP
5	03-004-3167(3SH.)	REF	SCHEMATIC DIAGRAM	
6				
7				
8				
9				
10	02-009-9200	1	CABLE SEMI-RIGID	
11	371.1000	1	LABEL SERIAL NO. TAG	
12	351.0024	1	CONN: BULKHEAD JACK SMS	
13				
14	378.1961	24"	WIRE NO. 30 AWG	
15	05.306-0607	1	REAR PANEL MODULE 5107	NOTE: ALL HARDWARE TO ASSEMBLE ITEMS 15 THRU 22, 30 & 31 TO BE PROVIDED BY INDUSTRIAL FAB. INC.
16	06.306-0607	REF	ARTWORK REAR PANEL "	
17	05-300-5107	1	FRONT PANEL MODULE 5107	

LEVEL 3

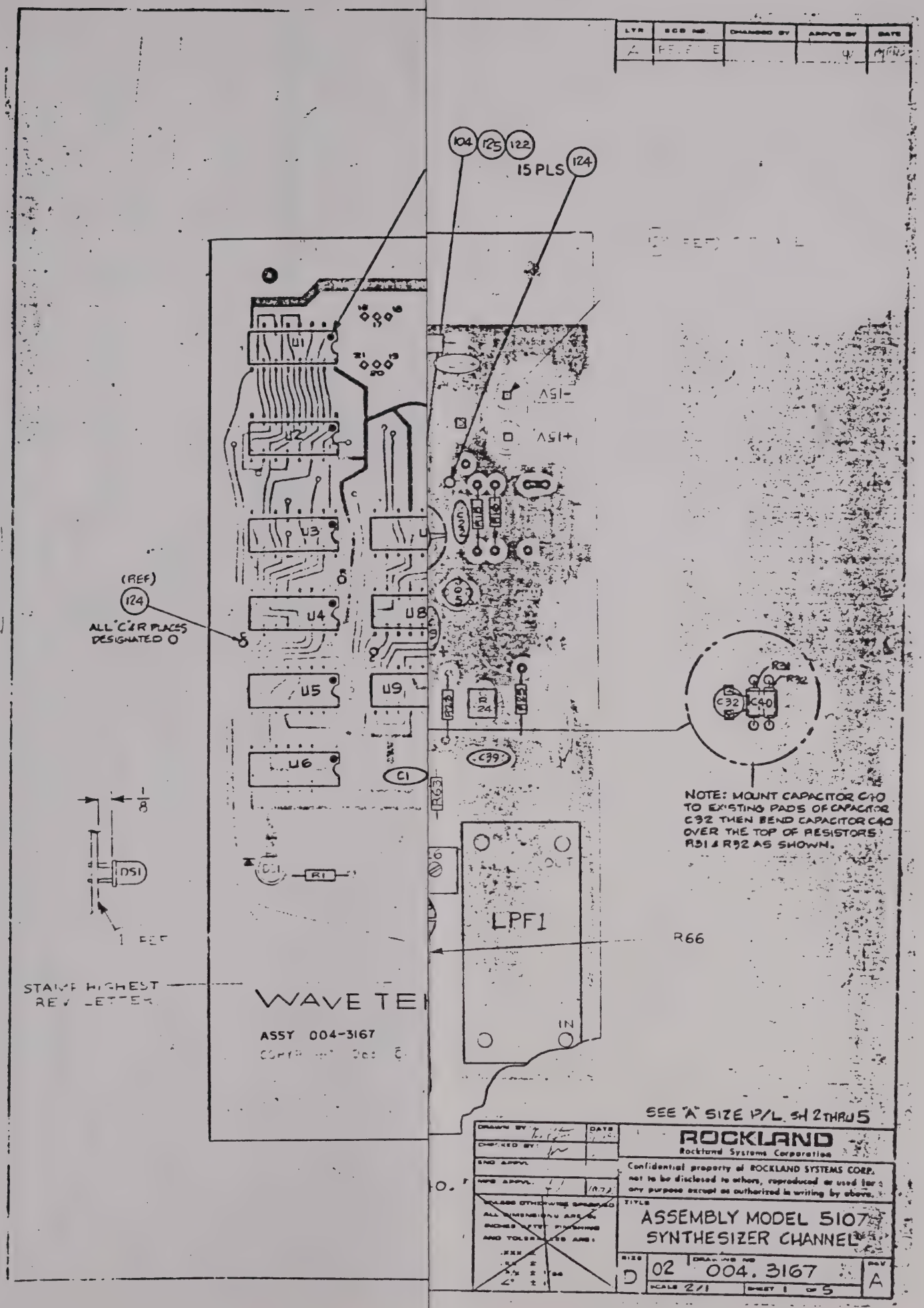
ROCKLAND
Rockland Systems Corporation

TITLE MODULE CHASSIS 5107 ASSEMBLY

LIST OF MATERIAL 02 002-3167 REV B

RELEASE AUTHORITY | CHK BY | ENGR | MFG | AUSY SIZE D | DATE 9/23/83 | SHEET 3 OF 3

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
18	06-300-5107	REF	ARTWORK FRONT PANEL 5107	
19	05-306-0916	1	MODULE CHASSIS RAIL R.H.(TOP)	
20	05-306-0914	1	MODULE CHASSIS RAIL L.H.(TOP)	
21	05-306-0103	2	MODULE CHASSIS PLATE TOP & BOTT	
22	05-306-0503	2	MODULE CHASSIS SIDE PANEL	
23	378.1745	3"	WIRE #24 AWG BOND YELLOW	
24	378.1755	3"	WIRE #24 AWG BOND GREEN	
25	367.6000	1	HOOD, CONNECTOR	
26	360.4041	6	SCREW, MACH. #4-40 B.H. .25LG	
27	388.1041	6	WASHER, LK EXT TOOTH NO.4	
28	388.0040	6	WASHER, FLAT NO.4	
29	387.4060	2	NUT, HEX NO.4-40 SM PATT	
30	05-306.0915	1	MODULE CHASSIS RAIL L.H(BOTT)	
31	05-306.0917	1	MODULE CHASSIS RAIL R.H.(BOTT)	
32	388.1042	2	WASHER, LK SPLIT NO.4	
33	381.4062	2	SCREW, MACH. NO 4-40 P.H. .38 LG	


104
125
122
15 PLS
124
U1
U2
U3
U4
U5
U6
U8
U9
-15V
+15V
(REF)
124
ALL C&R PLACES DESIGNATED O
C32
C40
R31
R32
NOTE: MOUNT CAPACITOR C40 TO EXISTING PADS OF CAPACITOR C32 THEN BEND CAPACITOR C40 OVER THE TOP OF RESISTORS R31 & R32 AS SHOWN.
C39
C1
R63
D1
R1
DS1
1/8
1 REF
LPF1
OUT
IN
R66
STAMP HIGHEST REV LETTER
WAVE TE
ASSY 004-3167
SEE "A" SIZE P/L SH 2 THRU 5
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ASSEMBLY MODEL 5107
SYNTHESIZER CHANNEL
SIZE D
02 004.3167
REV A
SCALE 2/1
SHEET 1 OF 5

LEVEL 3

ROCKLAND
Rockland Systems Corporation

TITLE MODULE CHASSIS 5107 ASSEMBLY

LIST OF MATERIAL 02 002-3167 REV B

RELEASE AUTHORITY | CHK BY | ASSY SIZE D | DATE 9/23/83 | SHEET 3 OF 3

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
18	06-300-5107	REF	ARTWORK FRONT PANEL 5107	
19	05-306-0916	1	MODULE CHASSIS RAIL R.H.(TOP)	
20	05-306-0914	1	MODULE CHASSIS RAIL L.H.(TOP)	
21	05-306-0103	2	MODULE CHASSIS PLATE TOP & BOTT	
22	05-306-0503	2	MODULE CHASSIS SIDE PANEL	
23	378.1745	3"	WIRE #24 AWG BOND YELLOW	
24	378.1755	3"	WIRE #24 AWG BOND GREEN	
25	367.6000	1	HOOD, CONNECTOR	
26	360.4041	6	SCREW, MACH. #4-40 B.H. .25LG	
27	388.1041	6	WASHER, LK EXT TOOTH NO.4	
28	388.0040	6	WASHER, FLAT NO.4	
29	387.4060	2	NUT, HEX NO.4-40 SM PATT	
30	05-306.0915	1	MODULE CHASSIS RAIL L.H (BOTT)	
31	05-306.0917	1	MODULE CHASSIS RAIL R.H.(BOTT)	
32	388.1042	2	WASHER, LK SPLIT NO.4	
33	381.4062	2	SCREW, MACH. NO 4-40 P.H. 38 LG	

DENOTES PIN 1 (TYP)

DENOTES WIRING POINTS

129 5 PLACES DESIGNATED □

78 120 127

101 125 122

104 125 122

15 PLS 124

1

(REF) 124 ALL 'C & R' PLACES DESIGNATED ○

STAMP HIGHEST REV. LETTER

WAVE TEK

ASSY 004-3167 REV A

74 119 126

121

NOTE: ADD IN TEST ONLY – C30, C31, C32, C40. (IF REQ.)

NOTE: MOUNT CAPACITOR C40 TO EXISTING PADS OF CAPACITOR C32 THEN BEND CAPACITOR C40 OVER THE TOP OF RESISTORS R91 & R92 AS SHOWN.

LPF1

R66

SEE 'A' SIZE P/L SH 2 THRU 5

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TITLE
ASSEMBLY MODEL 5107
SYNTHESIZER CHANNEL

SIZE D | 02 004.3167 | REV A

SCALE 2/1 SHEET 1 OF 5

ROCKLAND
Rockland Systems Corporation

TITLE: ASSY MODEL 5107 SYNTHESIZER CHANNEL

LIST OF MATERIAL: 02-004-3167 REV: A

RELEASE AUTHORITY | CHK BY | ENG RM | MFG | ASSY SIZE D | DATE 9/27/83 | SHEET 2 OF 5

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
1	01-320-3167	1	P.C. MAINBOARD (5107)	
2				
3				
4				
5	00-119-4990	1	R: FXD METFLM 49.9Ω 1% 1/8W	R9
6	00-110-1001	8	R: 100Ω 1/10W	R58, R56, R54, R52, R44, R42, R40, R18
7	00-110-1691	2	R: 169Ω	R33, R35
8	00-110-2001	2	R: 200Ω	R37, R38
9	00-110-5111	1	R: 511Ω	R36
10	00-110-5621	1	R: 562Ω	R60
11	00-110-7501	1	R: 750Ω	R63
12	00-110-7871	5	R: 787Ω	R28, R29, R30, R31, R32
13	00-110-8251	6	R: 825Ω	R46, R47, R48, R49, R50, R51
14	00-111-1181	1	R: 1.18K	R34
15	00-111-1501	1	R: 1.50K	R41
16	00-111-3091	1	R: 3.09K	R43
17	00-111-6341	1	R: 6.34K	R45
18	00-112-1271	1	R: 12.7K	R53
19	00-112-2551	1	R: 25.5K	R55
20	00-112-4991	1	R: 49.9K 1/10W	R57
21	00-111-1001	1	R: 1K 1/10W	R13
22	00-110-1150	1	R: FXD METFLM 115Ω 1% 1/8W	R25
23	00-116-0101	3	R: FXD COMP 10Ω 5% 1/4W	R11, R10, R39
24	00-116-0301	2	R: 30Ω	R61, R66
25				
26	00-116-0471	2	R: 47Ω	R8, R16
27				
28	00-116-0821	1	R: 82Ω	R23
29				
30	00-116-1161	1	R: 160Ω	R1
31	00-116-1181	1	R: 180Ω	R5
32	00-116-1221	2	R: 220Ω	R4, R64
33	00-116-1271	1	R: FXD COMP 270Ω 5% 1/4W	R62

ROCKLAND
Rockland Systems Corporation

TITLE: ASSY MODEL 5107 SYNTHESIZER CHANNEL

LIST OF MATERIAL: 02-004-3167 REV: A

RELEASE AUTHORITY: RM | ENG: [illegible] | ASSY SIZE: D | DATE: 9/27/83 | SHEET 3 OF 5

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
34				
35	00-116-1331	1	R: FXD COMP 330Ω 5% 1/4W	R65
36	00-116-1561	1	R: 560Ω	R15
37				
38	00-116-2101	4	R: 1.0K	R6, R3, R2, R67
39	00-116-2221	3	R: 2.2K	R22, R19, R14
40				
41	00-116-4101	1	R: FXD COMP 100K 5% 1/4W	R59
42	00-116-2471	1	R: FXD COMP 4.7K 5% 1/4W	R7
43				
44	00-118-1503	1	R: VAR. CMT 500Ω 3/8 SQ FM	R26
45	00-118-0500	1	R: VAR. CERMET 50Ω 5W	R24
46	00-118-1100	5	R: VAR. CERMET 100Ω 10% 1/2W	R72, R71, R70, R69, R68
47	00-118-2500	1	R: VAR. CERMET 5.0K 3/4 RECT	R21
48				
49	108-0180	3	C: VAR. MICA 3-18 PF	C30, C31, C32 } FOR INSERT IN TEST (IF REQ.)
50	106-0330	1	C: FXD CER 33PF 10% 200V	C40 } FOR INSERT IN TEST (IF REQ.)
51				
52	00-100-3105	2	C: FXD MONO .01μf +80-20% 50V	C24, C25
53	00-100-4102	14	C: FXD. MONO .1μf +80-20% 50V	C1, C2, C3, C4, C5, C6, C7, C10, C11, C12
54				C13, C35, C33, C34
55				
56	00-101-0100	1	C: FXD MICA DP 10PF 10% 500V	C41
57	00-101-1180	1	C: FXD MICA 180pf 10% 500V	C21
58	00-101-1820	2	C: FXD MICA 820pf 10% 500V	C18, C20
60	00-109-4100	4	C: FXD TANT .10μf 20% 35V	C16, C28, C29, C22
61	00-109-5100	2	C: TANT 1.0μf 20% 35V	C14, C15
62	00-109-6100	1	C: TANT 10μf 20% 35V	C19
63	00-109-6470	2	C: ELECT 47μf 40-63V	C26, C27
64	00-109-6680	2	C: FXD TANT 68μf 20% 6V	C8, C9
65	00-106-3470	1	C: FXD CERMLD .047μf 10% 200V	C36
66				

FORM NO 1004

ROCKLAND
Rockland Systems Corporation

TITLE ASSY MODEL 5107
SYNTHESIZER CHANNEL

LIST OF MATERIAL 02-004-3167 REV A

RELEASE AUTHORITY | CHG NTY | ENG RM | MFG QW | ASSY SIZE D | DATE 9/27/83 | SHEET 4 OF 5

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
67	00-101-2180	1	C: FXD MICA 1800pf 1% 500V	C39
68	00-101-1470	1	C: FXD MICA 470pf 10% 500V	C38
69	00-122-0106	8	U: INT CKT 74195	U4, U6, U8, U13, U20, U24, U27, U31
70	00-122-0131	4	U: 74367	U2, U11, U18, U33
71	00-122-7400	1	U: 7400	U38
72	00-122-7404	1	U: 7404	U54
73	00-122-7410	2	U: 7410	U39, U40
74	00-122-7437	1	U: 7437	U25
75	00-122-7440	2	U: 7440	U16, U45
76	00-122-7474	2	U: 7474	U48, U49
77	00-122-7483	12	U: 7483	U3, U5, U7, U9, U12, U19, U21, U23, U26, U28, U30, U34
78	00-122-9014	7	U: 9014	U15, U22, U29, U36, U41, U42, U43
79	00-123-7474	3	U: 74H74	U14, U35, U37
80	00-124-7474	6	U: 74S74	U50, U51, U52, U53, U55, U56
81	00-125-0109	4	U: INT CKT 74LS174	U1, U10, U17, U32
82	00-129-3000	1	U: ROM 512 X 8 (SIGNETICS)	U44
83	00-120-3529	1	U: VOLT COMP. LM361	U46
84	00-120-4830	1	U: DUAL LINE DRIVER 8830	U47
85				
86				
87	00-131-0200	1	CR: SIL ZENER 1N968B	CR6
88	00-131-9622	1	CR: SIL ZENER 1N5234	CR20
89	00-131-9621	1	CR: SIL ZENER 1N823	CR19
90	00-131-9680	2	CR: SIL ZENER 1N754	CR1, CR2
91	00-131-9872	1	CR: SIL ZENER 1N5238 2%	CR21
92	00-132-0457	3	CR: SIL LO LEAK	CR3, CR4, CR5
93	00-133-2800	11	CR: HOT CARRIER	CR8 THRU CR18
94	00-131-9562	1	CR: SIL ZN 5.6V 5% 1W 1N4734A	CR22
95				
96	00-171-1600	1	LED: RED 2MCD @ 10,40DVA	DS1
97				
98				
99				

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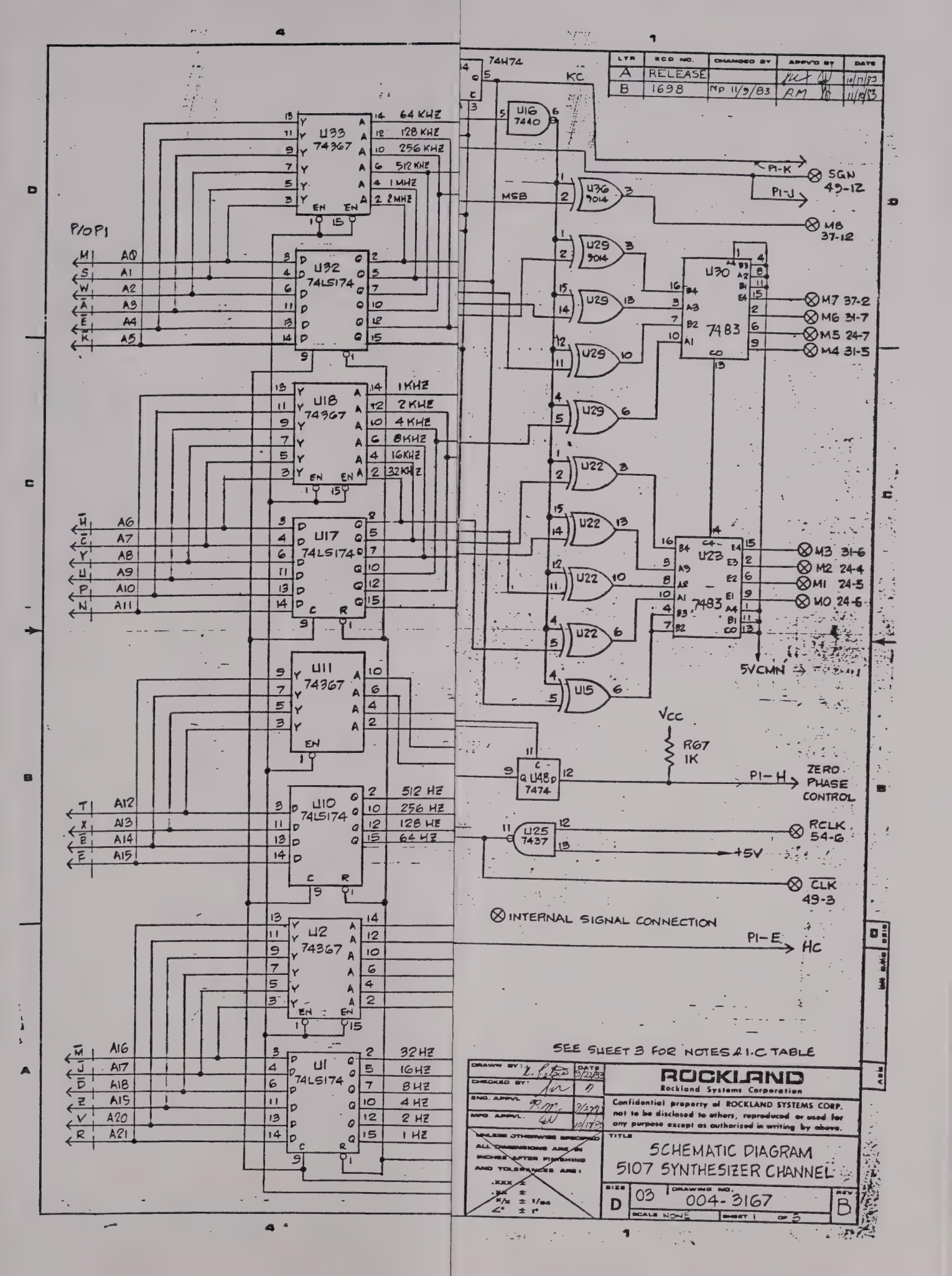
TITLE ASSY MODEL 5107 SYNTHESIZER CHANNEL

LIST OF MATERIAL 02-004-3167 REV A

RELEASE AUTHORITY | ENGRG | 2/9/83 | QA | ASSY SIZE D | DATE 9/27/83 | SHEET 5 OF 5

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
100	00-134-0065	1 PR	Q: SIL NPN MATCHED PAIR	Q1, Q4
101	00-134-2219	1	Q: SIL NPN (2N2219A)	Q2,
102	00-134 2222	3	Q: SIL NPN 2N2222A	Q17, Q18, Q5
103	00-136-4122	11	Q: SIL PNP 2N4122	Q6 THRU Q16
104	00-136-2905	1	Q: SIL PNP (2N2905A)	Q3
105				
106				
107				
108				
109				
110	00-150-1220	2	L: FXD 220uh ±10%	L3, L4
111	00-150-9151	1	L: FXD 1.5uh ±10%	L1
112	00-150-9220	1	L: FXD 2.2uh ±10%	L2
113				
114				
115				
116	00-165-3002	1	FILTER LOW PASS 0-3MHZ	LPF1
117				
118				
119	00-353-1403	2	SOCKET I.C. (14 PIN)	USED ON U25, U49
120	00-353-1604	3	SOCKET I.C. (16 PIN)	USED ON U41, U42, U43
121	00-353-2402	1	SOCKET I.C. (24 PIN)	USED ON U44
122	376-2108	2	SPACER: TXSTR LEAD, NYL, LOW	USE UNDER Q2, Q3
123	367-0413	1	HEAT SINK TO-18	MOUNTED ON Q18
124	00-354-0007	15	CONN. TERM. PIN WW.025 (2END)	
125	00-367-0400	2	HEAT SINK TO-8	USED ON Q2, Q3
126	00-368-5001	2	INSULATOR 14 PIN I.C.	USED ON U25, U49
127	00-368-5002	3	INSULATOR 16 PIN I.C.	USED ON U41, U42, U43
128				
129	00.354-0006	5	CONN TERM: .093 X .435	
130	00.378.1761	36"	WIRE # 24 AWG SOLID KYNAR BLUE	
131	00.995.0001	REF	INK SPEC. DRAWING	
132				

FORM NO. 3004



LTR	ECO NO.	CHANGED BY	APPVD BY	DATE
A	RELEASE			10/17/83
B	1698	MP 11/9/83	RM	11/16/83

DRAWN BY: L. Peters 9/22/83
CHECKED BY:
ENG. APPVL
MFG. APPVL

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE: .XXX ± .XX ± 1/64 X/X ± 1/64 ∠° ± 1°

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TITLE
SCHEMATIC DIAGRAM
5107 SYNTHESIZER CHANNEL

SIZE D | DRAWING NO. 004-3167 | REV B
SCALE NONE | SHEET 1 OF 3

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TITLE ASSY MODEL 5107 SYNTHESIZER CHANNEL

LIST OF MATERIAL 02-004-3167 REV A

RELEASE AUTHORITY | COPY | ASSY SIZE D | DATE 9/27/83 | SHEET 5 OF 5

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
100	00-134-0065	1 PR	Q: SIL NPN MATCHED PAIR	Q1, Q4
101	00-134-2219	1	Q: SIL NPN (2N2219A)	Q2,
102	00-134-2222	3	Q: SIL NPN 2N2222A	Q17, Q18, Q5
103	00-136-4122	11	Q: SIL PNP 2N4122	Q6 THRU Q16
104	00-136-2905	1	Q: SIL PNP (2N2905A)	Q3
105				
106				
107				
108				
109				
110	00-150-1220	2	L: FXD 220uh ±10%	L3, L4
111	00-150-9151	1	L: FXD 1.5uh ±10%	L1
112	00-150-9220	1	L: FXD 2.2uh ±10%	L2
113				
114				
115				
116	00-165-3002	1	FILTER LOW PASS 0-3MHZ	LPF1
117				
118				
119	00-353-1403	2	SOCKET I.C. (14 PIN)	USED ON U25, U49
120	00-353-1604	3	SOCKET I.C. (16 PIN)	USED ON U41, U42, U43
121	00-353-2402	1	SOCKET I.C. (24 PIN)	USED ON U44
122	376-2108	2	SPACER: TXSTR LEAD, NYL, LOW	USE UNDER Q2, Q3
123	367-0413	1	HEAT SINK TO-18	MOUNTED ON Q18
124	00-354-0007	15	CONN. TERM. PIN WW.025 (2END)	
125	00-367-0400	2	HEAT SINK TO-8	USED ON Q2, Q3
126	00-368-5001	2	INSULATOR 14 PIN I.C.	USED ON U25, U49
127	00-368-5002	3	INSULATOR 16 PIN I.C.	USED ON U41, U42, U43
128				
129	00.354.0006	5	CONN TERM: .093 X .435	
130	00378.1761	36"	WIRE # 24 AWG SOLID KYNAR BLUE	
131	00.995.0001	REF	JNK SPEC. DRAWING	
132				

FORM NO. 3004

LTR	ECO NO.	CHANGED BY	APPVD BY	DATE
A	RELEASE			10/1/83
B	1698	NP 11/9/83	AM	11/8/83

P/O P1

M1 A0
S A1
W A2
A A3
E A4
K A5

U33 74367 — 64 KHZ, 128 KHZ, 256 KHZ, 512 KHZ, 1 MHZ, 2 MHZ

U32 74LS174

H A6
C A7
Y A8
E A9
P A10
N A11

U18 74367 — 1 KHZ, 2 KHZ, 4 KHZ, 8 KHZ, 16 KHZ, 32 KHZ

U17 74LS174

U11 74367

T A12
X A13
B A14
E A15

U10 74LS174 — 512 HZ, 256 HZ, 128 HZ, 64 HZ

M A16
U A17
D A18
Z A19
V A20
R A21

U2 74367

U1 74LS174 — 32 HZ, 16 HZ, 8 HZ, 4 HZ, 2 HZ, 1 HZ

R2 1K → +5V

U36 9014 ×3

U34 7483 — 64 KHZ, 128 KHZ, 256 KHZ, 512 KHZ, 1 MHZ, 2 MHZ

U26 7483 — 1 KHZ, 2 KHZ, 4 KHZ, 8 KHZ, 16 KHZ, 32 KHZ

U19 7483

U12 7483 — Vcc

U7 7483 — 512 HZ, 256 HZ, 128 HZ, 64 HZ

U3 7483 — 32 HZ, 16 HZ, 8 HZ, 4 HZ, 2 HZ, 1 HZ

U28 7483 — Vcc

U21 7483

U9 7483 — Vcc

U5 7483 — HZ CARRY

KHZ CARRY

P/O P1

U5A 7404

F READ
N EN
L LOAD
P ACLK
S CLKR

U25 7437 ×2

U45 7440

RCLK

U11 74367 — ACKA, PRES

P/O P1 — 5V CMN

U14 74H74 — QUAD

U35 74H74 — SGN, MSB

U27 74195

U20 74195

U13 74195

U8 74195

U4 74195

U6 74195

U16 7440

U29 9014 ×4

U30 7483 — M7 37-2, M6 31-7, M5 24-7, M4 31-5

U22 ×4

U23 7483 — M3 31-6, M2 24-4, M1 24-5, M0 24-6

U15

5V CMN

KC

P1-K → SGN 49-12

P1-J → M8 37-12

U48 7474 — Vcc, RG7 1K, P1-H → ZERO PHASE CONTROL

U25 7437 — RCLK 54-G, +5V, CLK 49-3

⊗ INTERNAL SIGNAL CONNECTION

P1-E → Hc

SEE SHEET 3 FOR NOTES & I-C TABLE

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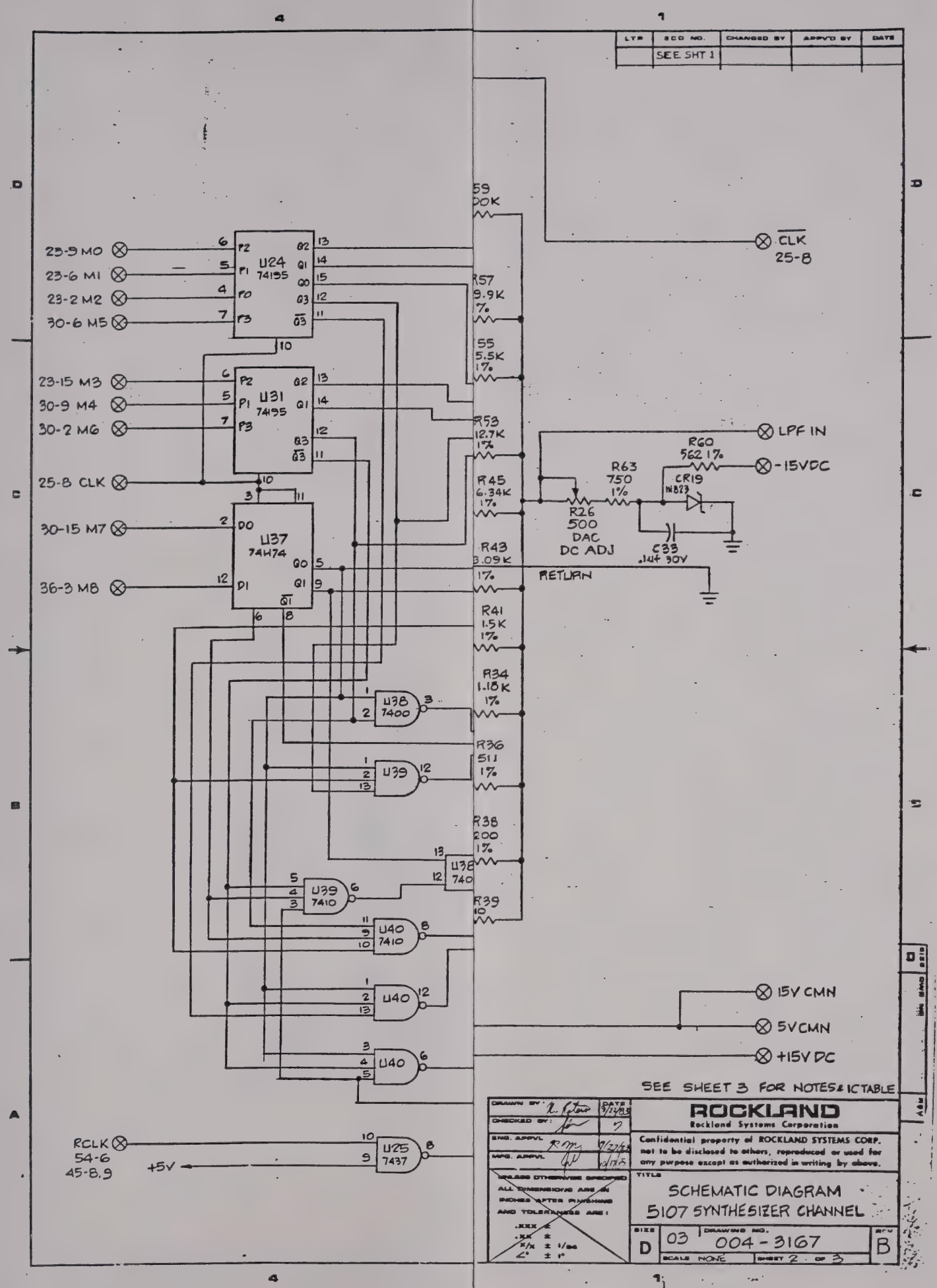
DRAWN BY: L. [illegible] DATE 9/26/83
CHECKED BY: [illegible]
ENG. APPVL: [illegible]
MFG APPVL: [illegible]

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE: .XXX ± .XX ± .X/.XX ± 1/64 ∠° ± 1°

TITLE
SCHEMATIC DIAGRAM
5107 SYNTHESIZER CHANNEL

SIZE D | DRAWING NO. 03 004-3167 | REV B
SCALE NONE | SHEET 1 OF 5


LTR | ECO NO. | CHANGED BY | APPVD BY | DATE
SEE SHT 1
23-9 M0
23-6 M1
23-2 M2
30-6 M5
U24 74155
23-15 M3
30-9 M4
30-2 M6
U31 74195
25-8 CLK
30-15 M7
36-3 M8
U37 74H74
R59 100K
R57 9.9K 1%
R55 5.5K 1%
R53 12.7K 1%
R45 6.34K 1%
R43 3.09K 1%
R41 1.5K 1%
R34 1.18K 1%
R36 511 1%
R38 200 1%
R39 10
CLK 25-8
LPF IN
R60 562 1%
-15VDC
R63 750 1%
CR19 IN823
R26 500 DAC DC ADJ
C33 .1uf 30V
RETURN
U38 7400
U39 7410
U40 7410
U40 740
U38 7400
U40 7410
U40 7410
U25 7437
RCLK 54-6 45-8,9
+5V
15V CMN
5VCMN
+15V DC
SEE SHEET 3 FOR NOTES & ICTABLE
DRAWN BY: R. Peters 9/24/73
CHECKED BY:
ENG. APPVL
MFG. APPVL
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER PLATING AND TOLERANCES ARE: .XXX ± .XX ± F/X ± 1/64 ∠° ± 1°
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TITLE
SCHEMATIC DIAGRAM
5107 SYNTHESIZER CHANNEL
SIZE D
03 004-3167
REV B
SCALE NONE
SHEET 2 OF 3

LTR	ECO NO	CHANGED BY	APPV'D BY	DATE
	SEE SHT 1			

D/A CONVERTER

23-9 MO
23-6 M1
23-2 M2
30-6 M5
23-15 M3
30-9 M4
30-2 M6
25-8 CLK
30-15 M7
36-3 M8

U24 74195 · U31 74195 · U37 74H74 · U44 ROM (MSB) · U38 7400 · U39 7410 · U40 7410 · U45 7440 · U25 7437

RCLK 54-6 45-8,9 · +5V · $\overline{CLK}$ 24-10 53-11

U43 9014 · U42 9014 · U41 · U53 74574 · U52 74574 · U51 74574 · U50 74574 · U56 74574 · U55 74574 · U49 7474

C95 .1uf 30V · C94 .1uf 30V

LSB · MSB

CR18 · CR17 · CR16 · CR15 · CR14 · CR13 · CR12 · CR11 · CR10 · CR9 · CR8

R51 825 1% · R50 825 1% · R49 825 1% · R48 825 1% · R47 825 1% · R46 825 1%

R68 100 · R28 787 10% · R69 100 · R29 787 10% · R70 100 · R30 787 10% · R31 787 10% · R71 100 · R72 100 · R32 787 10%

Q16 · Q15 · Q14 · Q13 · Q12 · Q11 · Q10 · Q9 · Q8 · Q7 · Q6

R59 100K · R58 100 1% · R57 49.9K 1% · R56 100 1% · R55 25.5K 1% · R54 100 1% · R53 12.7K 1% · R52 100 10% · R45 6.34K 1% · R44 100 1% · R43 3.09K 1% · R42 100 1% · R41 1.5K 1% · R40 100 1% · R34 1.18K 1% · R33 170 1% · R36 511 1% · R35 170 1% · R38 200 1% · R37 200 1% · R39 10

C30 3.5-18 PF · C31 3.5-18 PF · C32 3.5-18 PF · C40 33 PF

$\overline{CLK}$ 25-8

LPF IN

-15VDC

R60 562 1% · R63 750 1% · CR19 IN823 · R26 500 DAC DC ADJ · C33 .1uf 30V

RETURN

CR20 IN5234 · CR21 IN5238

Q17 2N2222 · Q18 2N2222 · RG4 220 · RG5 330 · RG1 30 · RG2 270

15V CMN · 5VCMN · +15V DC

SGN 35-9

C30, C31, C32 & C40 TO BE INSERTED IN TEST. (IF REQ.)

SEE SHEET 3 FOR NOTES & ICTABLE

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DRAWN R. Cyland 8/17/78 · CHECKED · ENG. APPVL. · MFG. APPVL.

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TITLE
SCHEMATIC DIAGRAM
5107 SYNTHESIZER CHANNEL

SIZE D · DRAWING NO. 03 004-3167 · REV B · SCALE NONE · SHEET 2 OF 3

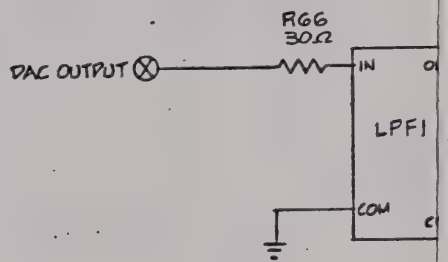
LTR	ECO NO.	CHANGED BY	APPVD BY	DATE
	SEE SHT 1			

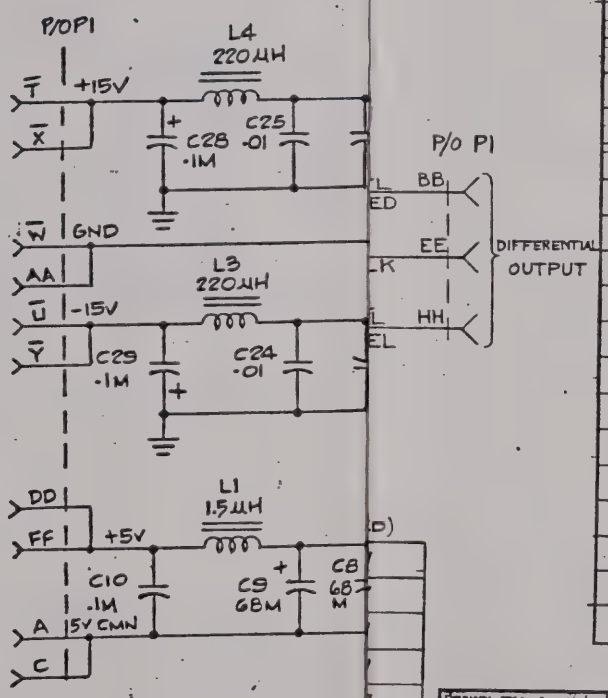
IED:
IN μf.
OHMS ¼W ±5%.

2N4122.

SHOWN.
TION

DESCRIPTION OF I.C'S			
IC NO.	PART NO.	PINS Vcc	PINS GND
3	122-7483	5	12
4	-0106	16	8,9
5	-7483	5	4,11,12,16
6	-0106	16	8,9
7	-7483	5	12
8	-0106	16	8,9
9	-7483	3,5,16	1,8,11,12
12	-7483	4,5	3,12,16
13	-0106	16	8,9
14	-7474	14	7
15	-9014	16	8
16	-7474	14,1,2,4	7
19	-7483	5	12
20	-0106	16	8,9
21	-7483	5	4,11,12,16
22	-9014	16	8
23	-7483	5	1,11,12,13
24	-0106	1,16	8,9
25	-7437	9,14,13	7
26	-7483	5	12
27	-0106	16	8,9
28	-7483	3,5,16	1,8,11,12
29	-9014	16	8
30	-7493	5	1,4,8,11,12
31	-0106	1,16	8,9
34	-7483	5	12
35	-7474	14	7
36	-9014	16	8
37	-7474	14	7
38	-7400	14	7
39	-7410	14	7
40	-7410	14	7
41	-9014	16	8
42	-9014	16	8
43	122-9014	16	8
44	129-3000	24	12,20





DRAWN BY: N. Estes	DATE 8/24/83	ROCKLAND Rockland Systems Corporation
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ENG. APPVL.		TITLE: SCHEMATIC DIAGRAM 5107 SYNTHESIZER CHANNEL
MFG. APPVL.		SIZE D · DRAWING NO. 004-3167 · REV B · SCALE · SHEET 3 OF 3

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE: .XXX ± .X ± X/x ± 1/64 ∠° ± 1°

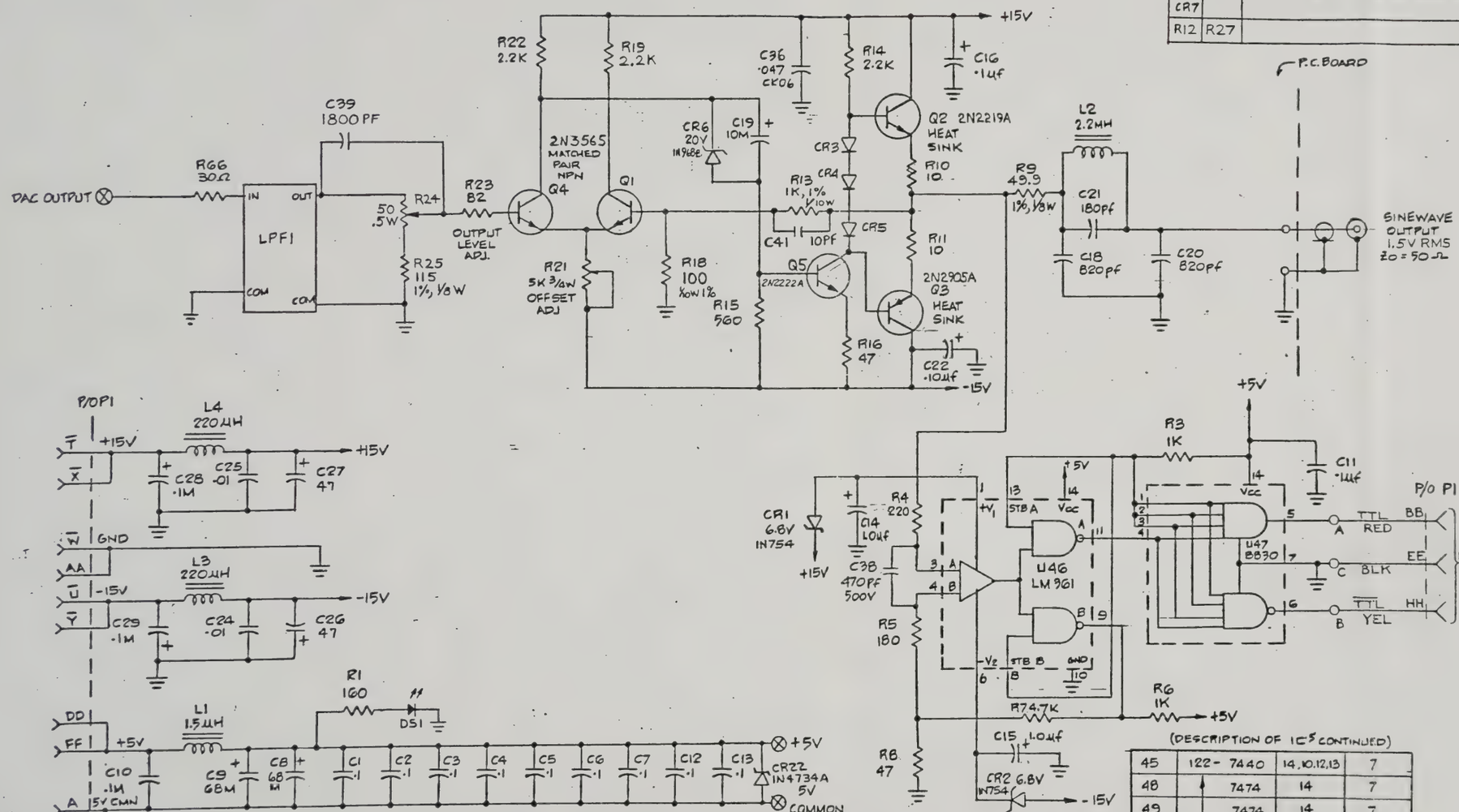
LTR	ECO NO	CHANGED BY	APPVD BY	DATE
	SEE SHT 1			

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL CAPACITOR VALUES ARE IN µf.
ALL RESISTOR VALUES ARE OHMS ½W ±5%.

TRANSISTORS ARE TYPE 2N4122.

ALL OTHER COMPONENTS AS SHOWN.
SEE TABLE FOR I.C. DESCRIPTION

REF DESIG NOT USED		
CR7		
R12	R27	



DESCRIPTION OF I.C'S			
IC NO.	PART NO.	PINS Vcc	PINS GND
3	122-7483	5	12
4	-0106	16	8,9
5	-7483	5	4,11,12,16
6	-0106	16	8,9
7	-7483	5	12
8	-0106	16	8,9
9	-7483	3,5,16	1,8,11,12
12	-7483	4,5	3,12,16
13	-0106	16	8,9
14	-7474	14	7
15	-9014	16	8
16	-7474	14,1,2,4	7
19	-7483	5	12
20	-0106	16	8,9
21	-7483	5	4,11,12,16
22	-9014	16	8
23	-7483	5	1,11,12,13
24	-0106	1,16	8,9
25	-7437	9,14,13	7
26	-7483	5	12
27	-0106	16	8,9
28	-7483	3,5,16	1,8,11,12
29	-9014	16	8
30	-7493	5	1,4,8,11,12
31	-0106	1,16	8,9
34	-7483	5	12
35	-7474	14	7
36	-9014	16	8
37	-7474	14	7
38	-7400	14	7
39	-7410	14	7
40	-7410	14	7
41	-9014	16	8
42	-9014	16	8
43	122-9014	16	8
44	129-3000	24	12,20

1	122-0109	16	8
2	122-0131	16	8
10	122-0109	16	8

11	122-0131	16	8
17	0109	16	8
18	0131	16	8
32	0109	16	8
33	122-0131	16	8
46	LM361	14	10
47	8830	14	7

(DESCRIPTION OF IC'S CONTINUED)

45	122-7440	14,10,12,13	7
48	7474	14	7
49	7474	14	7
50	7474	14	7
51	7474	14	7
52	7474	14	7
53	7474	14	7
55	7474	14	7
56	122-7474	14	7
54	122-7404	14	7

DRAWN BY: R. Peters 2/78
CHECKED BY: [illegible]
ENG. APPVL.
MFG. APPVL.

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Rockland Systems Corporation

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TITLE: SCHEMATIC DIAGRAM 5107 SYNTHESIZER CHANNEL

SIZE D | DRAWING NO. 004-3167 | REV B | SCALE — | SHEET 3 OF 3

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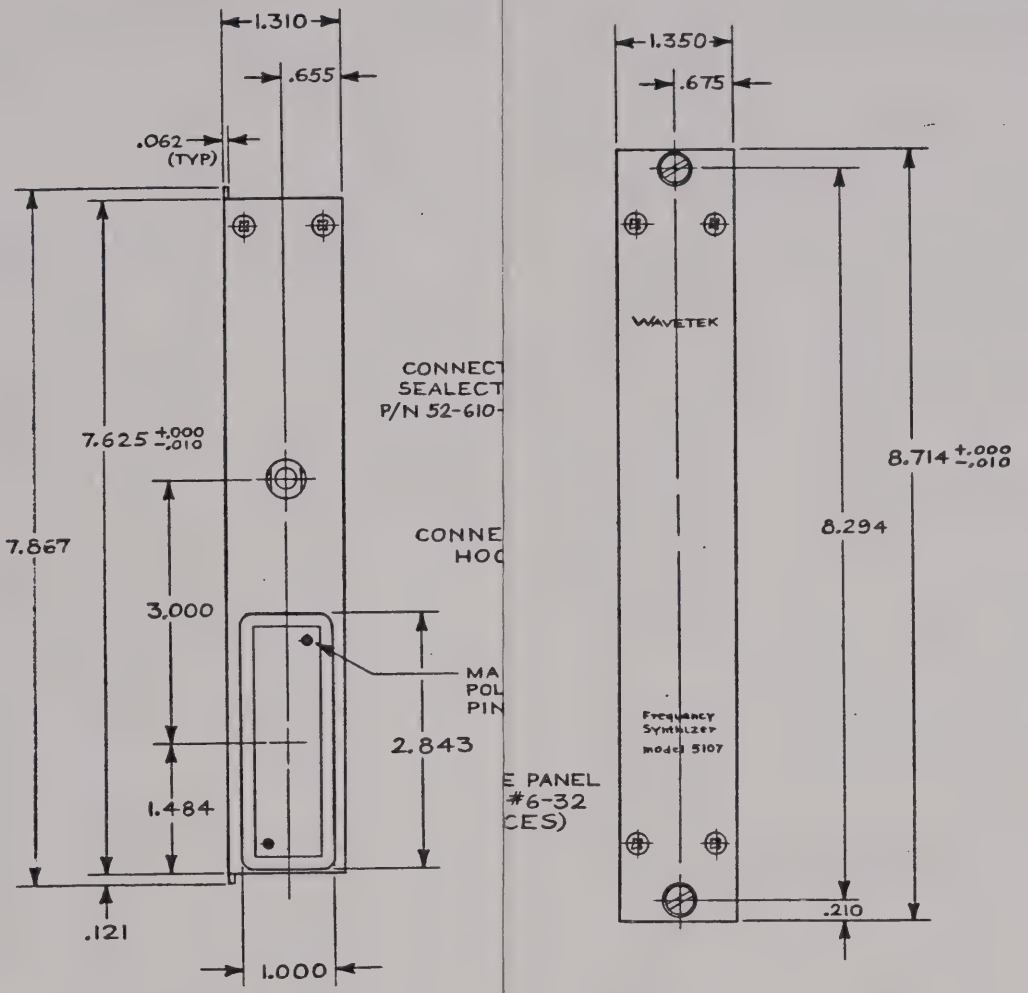
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A	RELEASE			10/10/83



NOTE:
1. TOP & BOTTOM CO

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

DRAWN	L. Peters	9/19/83
CHKD	[illegible]	"
ENG APPR.	[illegible]	9/19/83
MFG APPR.	[illegible]	10/10/83
ISSUED		

WAVETEK ROCKLAND Wavetek Rockland, Inc.

TITLE: OUTLINE
FREQUNCY SYNTHIZER
0-3 MHz

SIZE	MODEL NO.	DRAWING NO.	REV
D	5107	00-000-3167	A

SCALE: 1:1 | CODE IDENT 50621 | SHEET 1 OF 1

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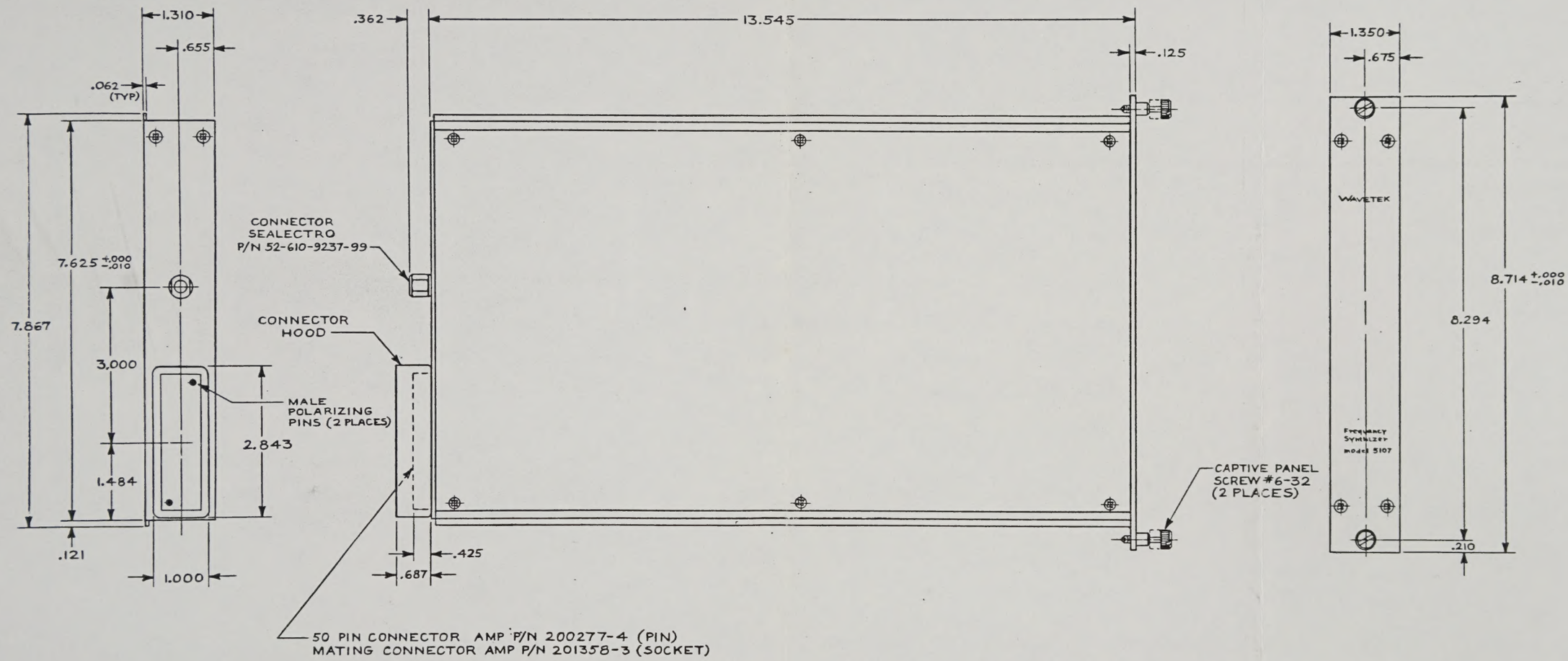
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A	RELEASE			10/17/83



NOTE:
1. TOP & BOTTOM COVERS ARE PERFORATED FOR VENTILATION.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
x/x ± 1/64 | .xxx ± .005 | .xx ± .01 | ∠ ±1°
MATERIAL: —
FINISH: —

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

		DATE
DRAWN	[illegible]	9/19/83
CHKD	[illegible]	"
ENG APPR.	[illegible]	9/19/83
MFG APPR.	[illegible]	9/19/83
ISSUED		

WAVETEK ROCKLAND Wavetek Rockland, Inc.

TITLE: OUTLINE FREQUNCY SYNTHIZER 0-3 MHz

SIZE	MODEL NO.	DRAWING NO.	REV
D	5107	00-000-3167	A

SCALE: 1:1 | CODE IDENT 50621 | SHEET 1 OF 1